

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	16	(repair same simulation) and (vhdl or verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:12
L2	6	("4717644"   "4758094"   "5598341"   "5686206"   "5994030"   "6483937").PN. OR ("6778695").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 21:18
L3	21	(fuse adj3 list)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:19
L4	6	3 and simulat\$7	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 21:19

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	vampire and opus and fuse	USPAT	OR	OFF	2005/06/15 20:31
L2	0	vampire and opus and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L3	0	vampire and opus	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L4	309	vampire	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:31
L5	0	4 and vhdl	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L6	0	4 and verilog	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L7	1	dracula and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:32
L8	45	("4618938"   "4706019"   "4721909"   "4837447"   "4895780"   "5065092"   "5198986"   "5251140").PN. OR ("5392222").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:34
L9	0	8 and fuse	USPAT	OR	OFF	2005/06/15 20:34
L10	4	8 and repair	USPAT	OR	OFF	2005/06/15 20:35
L11	1	verilog adj path	USPAT	OR	OFF	2005/06/15 20:36
L12	64	verilog same path	USPAT	OR	OFF	2005/06/15 20:36
L13	3	12 and fuse	USPAT	OR	OFF	2005/06/15 20:36

L14	7	("5970254"   "6006321"   "6028445"   "6150836"   "6182268"   "6311200").PN. OR ("6539477").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:39
L15	30	repair and (integrated adj circuit) and verilog	USPAT	OR	OFF	2005/06/15 20:39
L16	22	("4722084"   "4876685"   "5255227"   "5270974"   "5598373"   "5764577"   "5764878"   "5970000"   "6006311"   "6065134"   "6081910").PN. OR ("6181614"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:52
L17	2	(verif\$7 adj3 repair) and simulation and (vhdl or verilog)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:53
L18	15	("5381417"   "5383167"   "5557531"   "5634115"   "5648909"   "5650938"   "5805861"   "5850348"   "5995955"   "6026220"   "6026228").PN. OR ("6591402"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:54

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	verilog adj2 simulat\$5 adj2 netlist	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L2	1	verilog same (simulated adj2 netlist)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L3	1	(vhdl or verilog) same (simulated adj2 netlist)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 19:57
L4	3	("5732247"   "6167363"   "6208954").PN. OR ("6856950").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 19:58
L5	39	repair and fuse and simulation and (path adj2 data) and repair and verify	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/15 20:01
L6	1	("5764878").PN.	USPAT	OR	OFF	2005/06/15 20:03
L7	0	("mapsamefuse").PN.	USPAT	OR	OFF	2005/06/15 20:03
L8	157	map same fuse	USPAT	OR	OFF	2005/06/15 20:03
L9	1	8 and verilog	USPAT	OR	OFF	2005/06/15 20:04
L10	53	8 and (verify or verification)	USPAT	OR	OFF	2005/06/15 20:04
L11	29	10 and repair	USPAT	OR	OFF	2005/06/15 20:04
L12	16	("4051354"   "4648075"   "5058070"   "5379258"   "5644699"   "5764878"   "5781717"   "6141768").PN. OR ("6408401").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/15 20:10
L13	24	verilog adj netlist	USPAT	OR	OFF	2005/06/15 20:10
L14	0	13 and enumeration	USPAT	OR	OFF	2005/06/15 20:10
L15	1	13 and enum\$8	USPAT	OR	OFF	2005/06/15 20:11
L16	1	13 and repair	USPAT	OR	OFF	2005/06/15 20:11
L17	0	13 and fuse\$5	USPAT	OR	OFF	2005/06/15 20:11
L18	17	13 and simulation	USPAT	OR	OFF	2005/06/15 20:14
L19	569	(703/14).CCLS.	USPAT	OR	OFF	2005/06/15 20:14

L20	0	19 and fuse and repair	USPAT	OR	OFF	2005/06/15 20:14
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☐ 1. **Automatic formal verification of fused-multiply-add FPUs**

Jacobi, C.; Weber, K.; Paruthi, V.; Baumgartner, J.;  
Design, Automation and Test in Europe, 2005. Proceedings  
2005 Page(s):1298 - 1303 Vol. 2

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Results for "((fuse &lt;and&gt; verilog)&lt;in&gt;metadata)"

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**1. Architectural design of a fast floating-point multiplication-add fused unit using signed-digit addition**

Chen, C.; Chen, L.-A.; Cheng, J.-R.;  
Computers and Digital Techniques, IEE Proceedings-  
Volume 149, Issue 4, July 2002 Page(s):113 - 120

[AbstractPlus](#) | Full Text: [PDF](#)(595 KB) IEEE JNL

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**2. Architectural design of a fast floating-point multiplication-add fused unit using signed-digit addition**

Chichyang Chen; Liang-An Chen; Jih-Ren Cheng;  
Digital Systems, Design, 2001. Proceedings. Euromicro Symposium on  
4-6 Sept. 2001 Page(s):346 - 353

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- ☐ 1. **Predicting the Location and Number of Faults in Large Software Systems**  
Ostrand, T.J.; Weyuker, E.J.; Bell, R.M.;  
Software Engineering, IEEE Transactions on  
Volume 31, Issue 4, April 2005 Page(s):340 - 355  
[AbstractPlus](#) | Full Text: [PDF](#)(1304 KB) IEEE JNL
- ☐ 2. **From conventional control to autonomous intelligent methods**  
RayChaudhuri, T.; Hamey, L.G.C.; Bell, R.D.;  
Control Systems Magazine, IEEE  
Volume 16, Issue 5, Oct. 1996 Page(s):78 - 84  
[AbstractPlus](#) | Full Text: [PDF](#)(1328 KB) IEEE JNL
- ☐ 3. **Tools that bind: creating integrated environments**  
Sharon, D.; Bell, R.;  
Software, IEEE  
Volume 12, Issue 2, March 1995 Page(s):76 - 85  
[AbstractPlus](#) | Full Text: [PDF](#)(940 KB) IEEE JNL
- ☐ 4. **Tools to engineer new technologies into applications**  
Bell, R.; Sharon, D.;  
Software, IEEE  
Volume 12, Issue 2, March 1995 Page(s):11 - 16  
[AbstractPlus](#) | Full Text: [PDF](#)(924 KB) IEEE JNL
- ☐ 5. **Experimental 6-GHz frozen wave generator with fiber-optic feed**  
Thaxter, J.B.; Bell, R.E.;  
Microwave Theory and Techniques, IEEE Transactions on  
Volume 43, Issue 8, Aug. 1995 Page(s):1798 - 1804  
[AbstractPlus](#) | Full Text: [PDF](#)(644 KB) IEEE JNL
- ☐ 6. **High-voltage onsite commissioning tests for gas-insulated substations using UHF partial discharge detection**  
Bell, R.; Charlson, C.; Halliday, S.P.; Irwin, T.; Lopez-Roldan, J.; Nixon, J.;  
Power Delivery, IEEE Transactions on  
Volume 18, Issue 4, Oct. 2003 Page(s):1187 - 1191  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(229 KB) IEEE JNL
- ☐ 7. **Results of NSTX heating experiments**  
Mueller, D.; Ono, M.; Bell, M.G.; Bell, R.E.; Bitter, M.; Bourdelle, C.; Darrow, D.S.; Efthimion, P.C.;  
Fredrickson, E.D.; Gates, D.A.; Goldston, R.J.; Grisham, L.R.; Hawryluk, R.J.; Hill, K.W.; Hosea, J.C.;  
Jardin, S.C.; Ji, H.; Kaye, S.M.; Kaita, R.; Kugel, H.W.; Johnson, D.W.; LeBlanc, B.P.; Majeski, R.;  
Mazzucato, E.; Medley, S.S.; Menard, J.E.; Park, H.K.; Paul, S.F.; Phillips, C.K.; Redi, M.H.; Rosenberg,  
A.L.; Skinner, C.H.; Soukhanovskii, V.A.; Stratton, B.; Synakowski, E.J.; Taylor, G.; Wilson, J.R.;



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- ☐ 1. **On-chip repair and an ATE Independent fusing methodology**  
Cowan, B.; Farnsworth, O.; Jakobsen, P.; Oakland, S.; Ouellette, M.R.; Wheeler, D.L.;  
Test Conference, 2002. Proceedings. International  
7-10 Oct. 2002 Page(s):178 - 186  
[AbstractPlus](#) | Full Text: [PDF](#)(551 KB) IEEE CNF
- ☐ 2. **Ultraviolet laser repair of advanced semiconductor memory devices**  
Baird, B.W.; Nilsen, B.E.; Hainsey, R.F.; Ho Wai Lo;  
Lasers and Electro-Optics, 2001. CLEO '01. Technical Digest. Summaries of papers presented at the  
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6-11 May 2001 Page(s):230  
[AbstractPlus](#) | Full Text: [PDF](#)(144 KB) IEEE CNF
- ☐ 3. **Reliability and design qualification of a sub-micron tungsten silicide E-Fuse**  
Tonti, W.R.; Fifield, J.A.; Higgins, J.; Guthrie, W.H.; Berry, W.; Narayan, C.;  
Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International  
25-29 April 2004 Page(s):152 - 156  
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- ☐ 4. **Reliability of laser activated metal fuses in DRAMs**  
Arndt, K.; Narayan, C.; Brintzinger, A.; Guthrie, W.; Lachtrupp, D.; Mauger, J.; Glimmer, D.; Lawn, S.;  
Dinkel, B.; Mitwalsky, A.;  
Electronics Manufacturing Technology Symposium, 1999. Twenty-Fourth IEEE/CPMT  
18-19 Oct. 1999 Page(s):389 - 394  
[AbstractPlus](#) | Full Text: [PDF](#)(756 KB) IEEE CNF
- ☐ 5. **An on-chip self-repair calculation and fusing methodology**  
Anand, D.; Cowan, B.; Farnsworth, O.; Jakobsen, P.; Oakland, S.; Ouellette, M.R.; Wheeler, D.L.;  
Design & Test of Computers, IEEE  
Volume 20, Issue 5, Sept.-Oct. 2003 Page(s):67 - 75  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(298 KB) IEEE JNL
- ☐ 6. **Product specific sub-micron E-fuse reliability and design qualification**  
Tont, W.R.; Fifield, J.A.; Higgins, J.; Guthrie, W.H.; Berry, W.; Narayan, C.;  
Integrated Reliability Workshop Final Report, 2003 IEEE International  
20-23 Oct. 2003 Page(s):36 - 40  
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- ☐ 7. **Micro programmable built-in self repair for SRAMs**  
Zappa, R.; Selva, C.; Rimondi, D.; Torelli, C.; Crestan, M.; Mastrodomenico, G.; Albani, L.;  
Memory Technology, Design and Testing, 2004. Records of the 2004 International Workshop on  
9-10 Aug. 2004 Page(s):72 - 77  
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The Verilog netlist written is also broken and cannot be legally read > back in to ... "It can do off-chip test > with laser fuse-box repair at manufacture. ...

<http://www.deepchip.com/posts/0360.html> - 59k - [Cached](#) - [Similar pages](#)

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... At the program level, fuse repair may also require a wafer-cost adder associated ...

Entry & Verification Solution Active-HDL 6.3 supports mixed VHDL, Verilog, C/C++ ...

<http://www.eedesign.com/silicon/showArticle.jhtml?articleId=17408099&kc=6325> - 58k - [Cached](#) - [Similar pages](#)

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Laser and electrical fuse based repair increases the complexity of physical design

... The compiler outputs consist of behavioral models in Verilog or VHDL, ...

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## [MICROS SEMINAR](#) [distance: 0]

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## 1. An architecture for a verilog hardware accelerator

Burns, C.;  
Verilog HDL Conference, 1996. Proceedings., 1996 IEEE International  
26-28 Feb. 1996 Page(s):2 - 11

[AbstractPlus](#) | Full Text: [PDF](#)(704 KB) IEEE CNF

IEEE STD IEEE Standard



## 2. Logic simulation methods for longest path delay estimation

Maksimovic, D.M.; Litovski, V.B.;  
Computers and Digital Techniques, IEE Proceedings-  
Volume 149, Issue 2, March 2002 Page(s):53 - 59

[AbstractPlus](#) | Full Text: [PDF](#)(767 KB) IEEE JNL


## 3. A top down design environment for data-path design [FIR filter]

Yamazaki, T.; Kondo, Y.;  
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27 Sept.-1 Oct. 1993 Page(s):266 - 269

[AbstractPlus](#) | Full Text: [PDF](#)(280 KB) IEEE CNF


## 4. Property-specific testbench generation for guided simulation

Gupta, A.; Casavant, A.E.; Ashar, P.; Liu, X.G.; Mukaiyama, A.; Wakabayashi, K.;  
Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and  
the 15th International Conference on VLSI Design. Proceedings.  
7-11 Jan. 2002 Page(s):524 - 531

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